

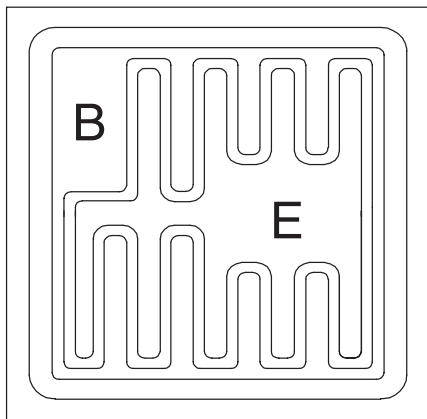
**PROCESS CP304**  
**Small Signal Transistor**  
NPN - High Current Transistor Chip

**Central**<sup>TM</sup>  
**Semiconductor Corp.**

**PROCESS DETAILS**

Process	EPITAXIAL PLANAR
Die Size	22 x 22 MILS
Die Thickness	9.0 MILS
Base Bonding Pad Area	5.7 X 4.0 MILS
Emitter Bonding Pad Area	5.3 X 4.0 MILS
Top Side Metalization	Al - 30,000Å
Back Side Metalization	Au - 18,000Å

**GEOMETRY**



BACKSIDE COLLECTOR R0

**GROSS DIE PER 4 INCH WAFER**

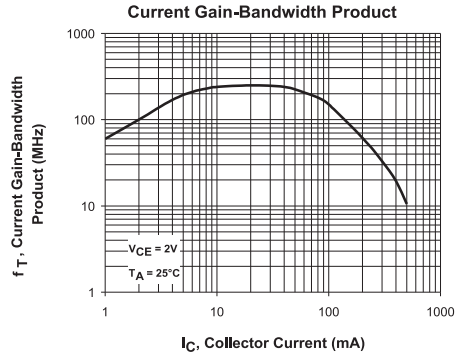
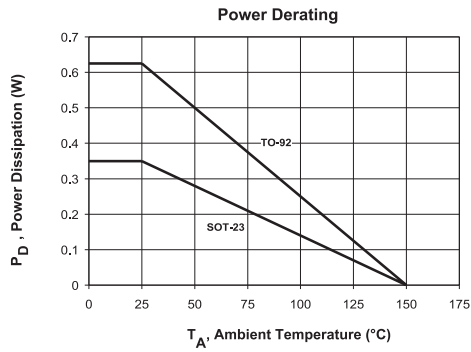
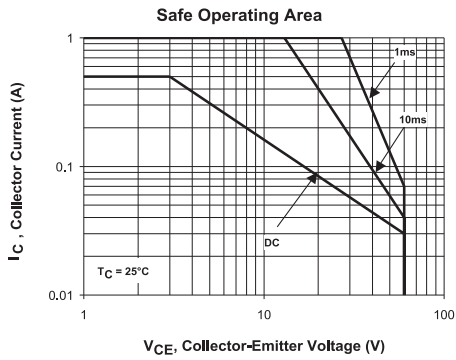
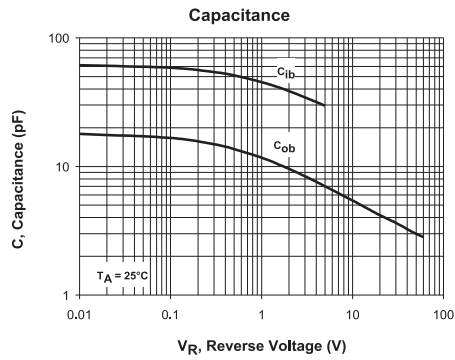
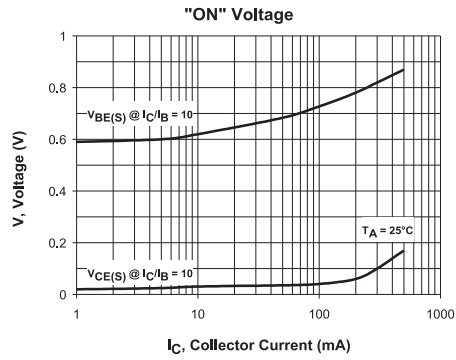
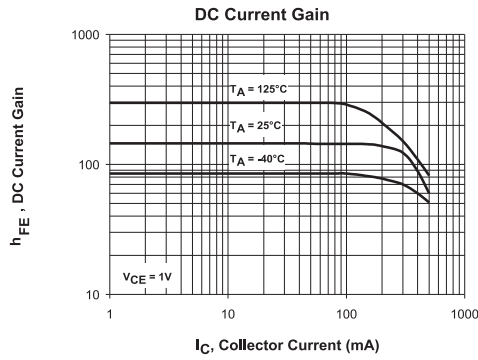
23,450

**PRINCIPAL DEVICE TYPES**

MPSA05  
MPSA06

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R3 (21-September 2003)



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